REMARKS

Amendments

Claims 1-17 are pending. Claims 1, 3, 4, 8 and 17 are amended herein. Claim 7 is cancelled.

Election/Restrictions – Examiner Interview Summary

A provisional restriction requirement was made on May 11, 2005 during a telephonic interview between Applicant's attorney and the Examiner.

Applicant hereby affirms the election of group I a (claims 1-17). The Applicant cancels groups Ib (claims 18-31), group Ic (claims 32-44), group Id (claims 45-59), group Ie (claims 60-67), group If (68-71), group II a (claims 72-78) and Group II b (Claims 79-87) without traverse, and reserves the right to reintroduce the claims in divisional applications at a later date.

Claim Rejections Under 35 U.S.C. § 112

Claims 3, 7 and 17 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses the rejection.

Applicant has amended claim 3 to correct the "and/or" logic as noted by the Examiner.

Also in regards to claim 3, the Examiner further maintains that "it is not how the first and second mask layer can be patterned with the same pattern. It is not clear how a pattern can be defined as the same pattern."

Claim 3, as amended, recites, "wherein patterning the first and second mask layers further comprises patterning the first and second mask layers with the same pattern." Applicant notes that it is well known in the art that mask layers are typically applied in semiconductor processing as a uniform layer and then patterned, generally by lithographic techniques, with a mask pattern to remove unwanted areas of the masking material, before further processing occurs. Applicant maintains that claim 3 states that the first and second mask layers are to be patterned to remove undesired portions of the first and second mask layers with the same pattern and that such would be apparent to one skilled in the art. Applicant also respectfully maintains that the relevant

features of the mask patterns of claim 3 are described, at least, by Figures 2B, and in Paragraphs [0045]-[0046] of the present Specification. In particular, the features of claim 3 of mask layer photoresist patterning are shown and described. Applicant thus contends that relevant features of claim 3 are definite and have been described in the specification to enable one skilled in the art to practice the invention.

Claim 7 has been cancelled herein.

The Examiner maintained, in regard to claim 17, that "[i]t is not clear how the second mask layer can expose a portion of the layer of dielectric when the second mask layer is formed overlying the layer of polysilicon wherein the layer of polysilicon overlying the layer of dielectric."

Claim 17, as amended, recites, "wherein patterning the first and second mask layers further comprises patterning the first mask layer to additionally expose a portion of the layer of dielectric over the drain region and patterning the second mask layer to expose a portion of the layer of polysilicon over the drain region." Applicant respectfully maintains that claim 17, as amended, recites patterning the second mask layer to expose a portion of the layer of polysilicon over the drain region, as noted by the Examiner. Applicant thus contends that relevant features of claim 17 are definite and are described in the specification to enable one skilled in the art to practice the invention.

Applicant therefore respectfully requests that the rejection of claims 3 and 17 under 35 U.S.C. § 112, second paragraph, be withdrawn in that the claims are not indefinite and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-9 and 12-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Patent No. 6,001,685) in view of Wu et al. (U.S. Patent No. 6,309,975). Applicant respectfully traverses this rejection and feels that claims 1-6, 8-9 and 12-17 are allowable for the following reasons.

Applicant respectfully maintains, that Kim teaches a method of making a self-aligned contact plug and coupled contact pad to a source that masks a dielectric layer and remove a portion from over a source region and sequentially deposits, masks and etches layers of differing conductive material to form a conductive plug contact to the source region. Applicant therefore respectfully maintains that the sections of Kim cited by the Examiner refers to the formation of conductive plugs, and thus does not disclose or suggest forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. The Applicant thus submits that the method of forming a contact plug of Kim does not correspond to Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Kim, Figure 6A-6I, Column 5, line 66 to Column 7, line 32.

In addition, Applicant maintains that Wu et al. discloses a method for masking and ion implanting layers of silicon based materials so that they can be selectively etched to preferentially remove the non-implanted portion. Applicant has also carefully reviewed Wu et al. and has found no mention of forming a trench shaped local interconnect by forming a trench shaped region in a dielectric layer, depositing a layer of polysilicon, masking the layer of polysilicon, selectively ion implanting the masked layer of polysilicon so that it can be selectively etched to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region. Applicant therefore respectfully maintains that Wu et al. also does not teach or suggest Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Wu et al., Column 10, line 51 to Column 27, line 20. Therefore combining the elements of Kim with Wu et al. does not teach or suggest a forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. Applicant therefore respectfully submits that Kim and Wu et al. do not teach or suggest all elements of the Applicant's claimed invention, either alone or in combination.

Applicant's claim 1, as amended, recites, in part, "removing a portion of the exposed portion of the layer of dielectric material to form a trench shaped region and expose the source region," and "forming a layer of polysilicon overlying the layer of dielectric material and trench

shaped region that is in contact with the exposed source region; forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the trench shaped region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region." As detailed above, Applicant submits that Kim and Wu et al. fail to teach or suggest such a method. As such, Kim and Wu et al. fail to teach or suggest all elements of independent claim 1. The Applicant therefore maintains that claim 1 is thus allowable over Kim and Wu et al., either alone or in combination.

Applicant respectfully contends that claim 1 has been shown to be patentably distinct from the cited reference. Claim 7 has been cancelled herein. As claims 2-6, 8-9 and 12-17 depend from and further define claim 1, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-6, 8-9 and 12-17.

Claims 1-2 and 4-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jenq et al. (U.S. Patent No. 6,159,788) in view of Wu et al. (U.S. Patent No. 6,309,975). Applicant respectfully traverses this rejection and feels that claims 1-2, 4-6 and 8-15 are allowable for the following reasons.

Applicant respectfully maintains, that Jenq et al. teaches a method of making an electrode for a DRAM charge storage capacitor that sequentially deposits, masks and etches a layers of conductive material to form an electrode for a DRAM charge storage capacitor that is in contact with a source/drain region and not the formation of a local interconnect. Applicant therefore respectfully maintains that the sections of Jenq et al. cited by the Examiner thus does not disclose or suggest forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. The Applicant thus submits that the method of forming an electrode for a DRAM charge storage capacitor of Jenq et

al. does not correspond to Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Jenq et al., Figure 4, Column 6, lines 30-64.

In addition, Applicant maintains, as stated above, that Wu et al. discloses a method for masking and ion implanting layers of silicon based materials so that they can be selectively etched to preferentially remove the non-implanted portion and does not disclose or suggest forming a trench shaped local interconnect by forming a trench shaped region in a dielectric layer, depositing a layer of polysilicon, masking, selectively ion implanting, and then selectively etching to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region. Applicant therefore respectfully maintains that Wu et al. also does not teach or suggest Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Wu et al., Column 10, line 51 to Column 27, line 20. Therefore combining the elements of Jenq et al. with Wu et al. does not teach or suggest a forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. Applicant therefore respectfully submits that Jenq et al. and Wu et al. do not teach or suggest all elements of the Applicant's claimed invention, either alone or in combination.

Applicant's claim 1, as amended, recites, in part, "removing a portion of the exposed portion of the layer of dielectric material to form a trench shaped region and expose the source region," and "forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region that is in contact with the exposed source region; forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the trench shaped region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region." As detailed above, Applicant submits that Jenq et al. and Wu et al. fail to teach or suggest such a method. As such, Jenq et al. and Wu et al. fail to teach or suggest all elements of independent claim 1. The

Applicant therefore maintains that claim 1 is thus allowable over Jenq et al. and Wu et al., either alone or in combination.

Applicant respectfully contends that claim 1 has been shown to be patentably distinct from the cited reference. Claim 7 has been cancelled herein. As claims 2, 4-6 and 8-15 depend from and further define claim 1, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-2, 4-6 and 8-15.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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